**Tutorial 3B: WRES1201 Computer System Architecture**

1. What general categories of function are specified by computer instruction?
2. List and briefly define the possible states that define an instruction execution?
3. List and briefly define two approaches to dealing with multiple interrupts.
4. What type of transfers must a computer's interconnection structure support? (e.g., bus)
5. What is the benefit of using a multiple-bus architecture compared to a single-bus architecture?

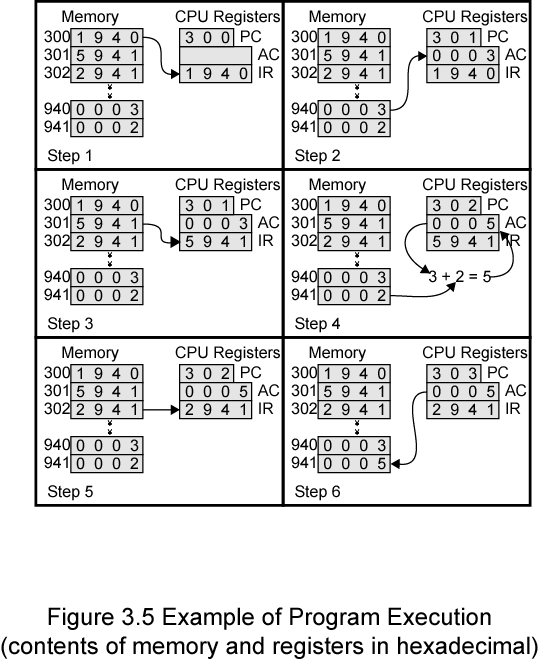


Figure 1

1. The program execution of Figure 1 is describe in the text using six steps. Expand this description to show the use of the MAR and MBR.
2. Consider a 32-bit microprocessor, with 16-bit external data bus, driven by a 16-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s?

**Individual Task**

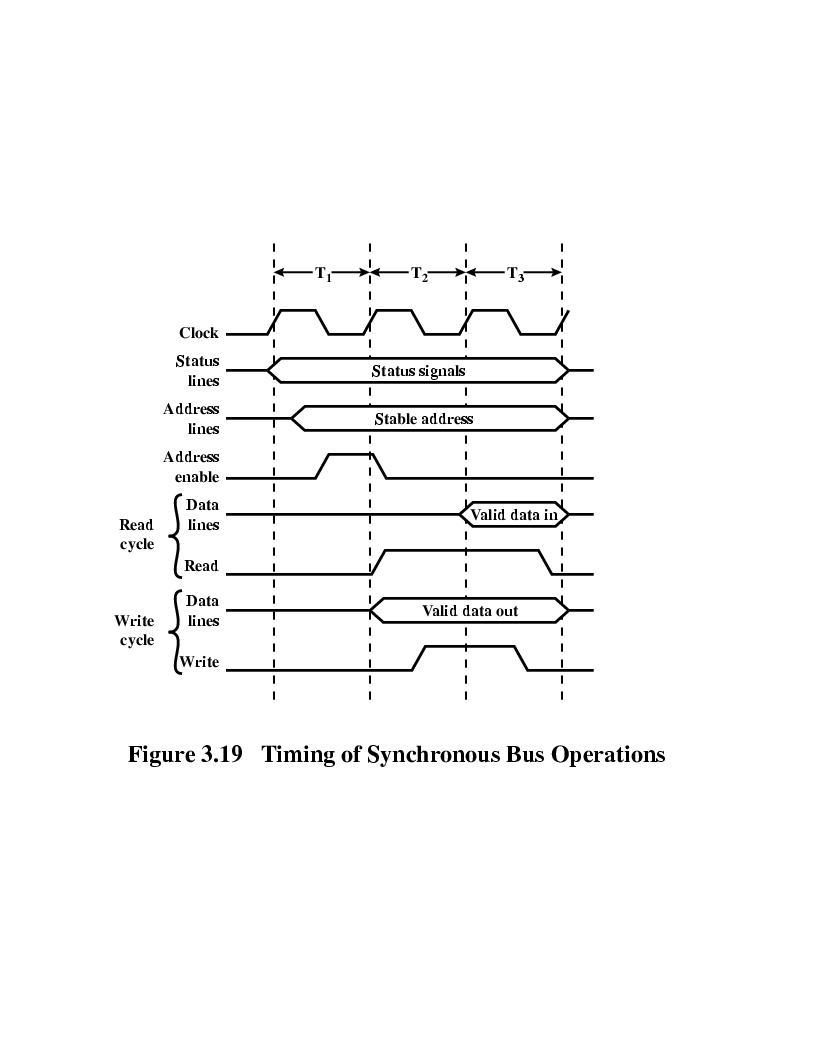


Figure 2

1. The Intel 8088 microprocessor has a read bus timing similar to that of Figure 2, but requires four processor clock cycles. The valid data is on the bus for an amount of time that extends into the fourth processor clock cycle. Assume a processor clock rate of 8MHz.
   1. What is the maximum data transfer rate?
   2. Repeat bur assume the need to insert one wait state per byte transferred.
2. Draw and explain a timing diagram for PCI write operation (similar to Figure 3)

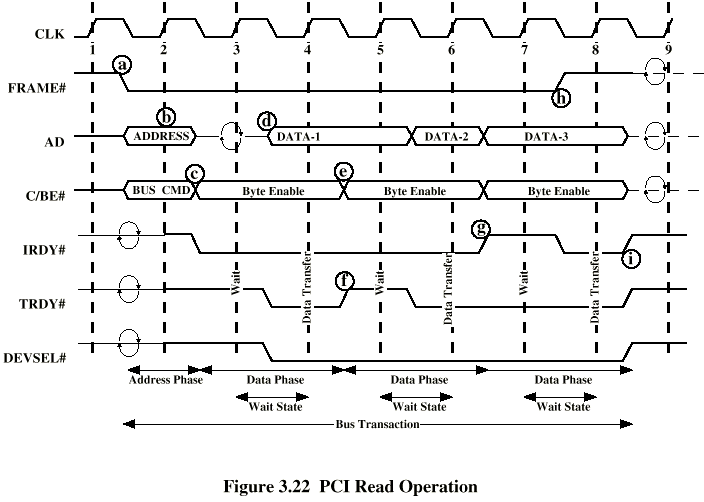


Figure 3